

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Jun Koyama et al. Art Unit : 2629
Patent No. : 7,224,339 Examiner : Kent Chang
Issue Date : May 29, 2007
Serial No. : 09/923,433
Filed : August 8, 2001
Title : LIQUID CRYSTAL DISPLAY DEVICE, METHOD OF DRIVING THE SAME,
AND METHOD OF DRIVING A PORTABLE INFORMATION DEVICE
HAVING THE LIQUID CRYSTAL DISPLAY DEVICE

Attn.: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box J450
Alexandria, VA 22313-1450

TRANSMITTAL OF REQUEST FOR CERTIFICATE OF CORRECTION

Applicants hereby request that a certificate of correction be issued for the above patent in accordance with the attached request.

The following references were considered by the Examiner on January 3, 2004 as evidenced by the attached initialed form PTO-1449.

2002/0018029 A1	2/14/2002	Koyama
2002/0021295 A1	2/21/2002	Koyama et al.
2002/0024054 A1	2/28/2002	Koyama et al.
2002/0024485 A1	2/28/2002	Koyama
2002/0036604 A1	3/28/2002	Yamazaki et al.

U.S. Patent No. 5,959,598, issued 9/28/1999 (McKnight) was cited by the Examiner in the office action mailed July 28, 2004 (copy attached).

Further, references EP 139 327 and JP 410253941 should be corrected, as they were improperly printed on the patent. EP 139 327 should be listed as EP I 139 327, as identified on the attached initial form PTO-1449 and JP 410253941 is incorrectly printed on the notice of references cited (PTO-892).

All errors sought to be corrected were made in printing by the Patent and Trademark Office, and no fee is believed to be due.

Applicant : Jun Koyama et al.
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Page : 2 of 2

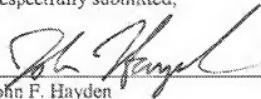
Attorney's Docket No.: 12732-064001 / US5158/5166

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date:

9/13/07


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CERTIFICATE OF CORRECTION**

Page 1 of 1

PATENT NO. :: 7,224,339
APPLICATION NO :: 09/923,433
DATED :: MAY 29, 2007
INVENTOR(S) :: SHUNPEI YAMAZAKI ET AL.

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On page 2, "U.S. PATENT DOCUMENTS", please add the following list of references that were omitted from the patent:

5,959,598	9/28/1999	McKnight
2002/0018029 A1	2/14/2002	Koyama
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2002/0024054 A1	2/28/2002	Koyama et al.
2002/0024485 A1	2/28/2002	Koyama
2002/0036604 A1	3/28/2002	Yamazaki et al.

On page 2, "FOREIGN PATENT DOCUMENTS", please correct the following references as indicated below:

EP	<u>1</u> 139 327	10/2001
JP	<u>410253941</u> <u>10-253941</u> A1	9/1998

MAILING ADDRESS OF SENDER:

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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 12732-064001	Application No. 09/923,433
Information Disclosure Statement by Applicant <i>(S)</i> (Use several sheets if necessary)		Applicant Jun Koyama et al.	
		Filing Date August 8, 2001	Group Art Unit 2673

JUN 03 2003
USPTO-98(b)

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AF							
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Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Désig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes No
AL							RECEIVED
AM							JUN 04 2003
AN							
AO							Technology Center 2600
AP							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Désig. ID	Document
	AQ	
	AR	
	AS	
	AT	

Examiner Signature <i>Anne Moyer</i>	Date Considered <i>1/3/04</i>
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 5,8,10,11,33,37,47,48,53,54,70-78,80-81 are rejected under 35 U.S.C. 103(a) as being unpatentable over **McKnight [5,959,598]**.

As to claims 5,8,33,37,47,48,53,54,70-72,74-76 80,81 **McKnight**, discloses a liquid crystal display device comprising pixels, wherein each of said pixels has n x m memory circuits (see, fig.8 (805) "storage capacitor"), n gate signal lines (fig.8 (779)"gate wire"), n Tufts having gate electrodes, source region and a drain region (fig.8 (781) "TFT"), wherein each of said gate electrodes is connected to a corresponding one of said gate signal lines (fig.8 (781) gate electrodes connected to gate lines (779)).

McKnight did not expressly detailed having a D/A converter for converting n bit digital signals stored in said n x m memory circuits into analog signals. However, **McKnight** in fig.11 clearly teaches an alternative way of arranging an LCD pixels in which a each pixels having a D/A converter (fig.11 (1014)) for converting n bit digital signals stored in n x m memory circuits (fig.11 (1005) into analog signals (col.20, lines 29-39). It would have been obvious to one skill in the art at the time of the invention was made to have been motivated to have incorporate **McKnight**'s D/A into LCD pixels with TFT and a memory system arrangement since this will allow to convert the digital display data into an analog signal data which will drives the pixels to the desired voltage.

Sheet (c)
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Page 2

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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 12732-064001	Application No. 09/923,433
Information Disclosure Statement by Applicant (Use several sheets if necessary)		Applicant Jun Koyama et al.	
(37 CFR 61.98(b))		Filing Date August 8, 2001	Group Art Unit 2629

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							Yes	
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Examiner Signature <i>Kent C. L.</i>	Date Considered 3/26/07
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Sheet (E)

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Examiner Amare Mengistu		Art Unit 2673	Page 1 of 1	

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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a))

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Sheet (E)

(19) 日本国特許庁 (JP)

(12) 公開特許公報 (A)

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G 0 2 F 1/133
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(54) 【発明の名称】 マトリクス型画像表示装置

(57) 【要約】

【課題】 短い表示信号入力時間の間でも各画素に高解像度の表示信号を入力することができ、高解像度の大形マトリクス型表示装置を提供すること。

【解決手段】 各表示画素回路1-4は、DA変換器2-2を備え、DA変換器2-2の出力にはTN液晶静電容量2-3が接続され、入力にはラッチ2-1の出力が接続されている。ラッチ2-1のタイミング入力はゲート線1-1を介してY駆動回路1-5に接続され、ラッチ2-1のデータ入力はデータバス1-2を介してX駆動回路1-6に接続されている。TN液晶静電容量2-3の他端部は共通電極2-4に接続されている。Y駆動回路1-5は、削側回路1-9から入力されるクロック1-7に従い、順次各行のゲート線1-1を選択して高電圧レベルに設定する。X駆動回路1-6にはデジタル表示信号がデジタル入力線1-8を経由して入力されており、一行分のデジタル表示信号が挿した時点で、各列毎にデータバス1-2に出力される。

